HIGH-PERFORMANCE DESIGNSYNC 2025

Semiconductor Engineer Powered by 3DEXPERIENCE

Hyatt Regency, Santa Clara, CA | USA

Rooms: Napa I, II, III

Date: September 24, 2025

Time: 08:30 AM (PDT)

Updated agenda!

Conference Agenda

08:30	Guest Check-in, Light Breakfast, and Networking	-
09:15	Welcome and Opening Remarks	Thai Do
09:30	Keynote Address by Cadence Design Systems: AI and Analog Design: Friends or Foes?	Steven Lewis
10:15	Unleashing Semiconductor Innovation through Strategic IP Generation, Management, and Reuse	John Maculley
11:00	Accelerating Semiconductor Innovation and Ecosystem Collaboration with 3DS Solutions	Bill Ruccio
12:00	Lunch Buffet and Networking	-
13:00	Live Demonstration of Semiconductor Engineer	Janet Barba; Bijan Dorostkar
14:00	Semiconductor Engineer Answers 5 Trends and 5 Challenges at 10x Performance	Dean Popowski
14:30	DesignSync and Semiconductor Engineer Deployment Options	Dean Popowski
14:45	Ask the Experts of Semiconductor Engineer	Sarah Ahmad; Bijan Dorostkar
15:15	Afternoon Refreshments and Networking	-
15:45	Ask the Experts of DesignSync	Marcia Tomseth; Janet Barba
16:15	Customer Roundtable and Discussion	-
17:00	Wrap-up and Closing Remarks	Thai Do
17:15	Evening Cocktails and Networking	-

Additional Information

Sessions and times are subject to change. To download the latest agenda, visit the event site at https://events.3ds.com/designsync-user-meeting-2025 or scan the QR code above.

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